

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10750714
	Filing Date		2003-12-31
	First Named Inventor	Gonzalez	
	Art Unit	2181	
	Examiner Name	Benjamin P. Geib	
	Attorney Docket Number	PA2683US	

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	3	6557092		2003-04-29	Callen	
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	6	6721866		2004-04-13	Roussel	
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	8	6732354		2004-05-04	Ebeling	

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	9	6744274		2004-06-01	Arnold	
	10	6795900		2004-09-21	Miller	
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	20	6986127		2006-01-10	Newlin	
	21	6996709		2006-02-07	Arnold	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	0 507 507	EP		1992-07-10	American Telephone		<input type="checkbox"/>
	2	0 668 659	EP		1995-08-23	Pilkington Germany		<input type="checkbox"/>
	3	1 443 417	EP		2004-08-04	ST Microelectronics		<input type="checkbox"/>

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4	152355	TW		2002-07-10	Adaptive Silicon, Inc.		<input type="checkbox"/>
5	152994	TW		2002-07-22	Adaptive Silicon, Inc.		<input type="checkbox"/>
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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	RUPP et al.; U.S. Patent Application No. 10/746,018, entitled "Architecture and Method for Reconfigurable Data Path Processing," filed Dec. 23, 2003.	<input type="checkbox"/>
	2	BECHADE, R.A. et al., "Programmable Arithmetic/Logic Circuits," IBM Technical Disclosure Bulletin, U.S. IBM Corp., New York, Vol. 3, No. 11, April 1981, pp. 4870-4873, XP-000713711.	<input type="checkbox"/>
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	5	DEHON, ANDRE, "Transit Note #118 Notes on Coupling Processors with Reconfigurable Logic," M.I.T. Transit Project, Last Updated March 21, 1995.	<input type="checkbox"/>
	6	DINIZ, et al., "Automatic Synthesis of Data Storage and Control Structures for FPGA-based Computing Engines," 2000, IEEE, pp 91-100.	<input type="checkbox"/>

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7	GONZALEZ, RICARDO E., "Xtensa: A Configurable and Extensible Processor," March-April 2000, IEEE Micro, pp 60-70.	<input type="checkbox"/>
8	HENNESSY, JOHN L. and DAVID A. PATTERSON, "Computer Organization and Design: The Hardware/Software Interface," 1998, 2nd edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, p. 345.	<input type="checkbox"/>
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11	JACOB et al; " Memory Interfacing and Instruction Specification for Reconfigurable Processors," 1999; ACM.	<input type="checkbox"/>
12	MIPS Technologies, Inc., "MIPS Extension for Digital Media with 3D," 1996, pp. 1-26.	<input type="checkbox"/>
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14	TANENBAUM, ANDREW S., "Modern Operating Systems," 2001, 2nd edition, Prentice Hall, New Jersey, p. 31.	<input type="checkbox"/>
15	TAYLOR, MICHAEL BEDFORD, et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," Microarchitecture, IEEE Micro, March-April 2002, pp 25-35.	<input type="checkbox"/>
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17	YE, Z.A. et al., "CHIMAERA: A high-performance architecture with a tightly-coupled reconfigurable functional unit," June 10-14, 2000, Proc. of the 27th International Symposium on Computer Architecture, pp. 225-235.	<input type="checkbox"/>

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	18	http://www.tensilica.com/products/xtensa_overview.htm Xtensa Processor Overview	<input type="checkbox"/>
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